Cryogenic etching of silicon with $SF_6/O_2/SiF_4$ plasmas: a modelling and experimental study

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Abstract: Cyrogenic etching of silicon is envisaged to enable better control over plasma processing in microelectronics and to limit plasma induced damage for features beyond the 14 nm technology node. We here present results of plasma modelling for a $SF_6/O_2/SiF_4$ plasma and of molecular dynamics (MD) simulations for predicting surface interactions, together with results of etch experiments for validation.

Keywords: plasma, etching, cryogenic, silicon, simulation

1. Introduction

Plasmas are widely used in the microelectronics industry for the fabrication of computer chips, during plasma etching and deposition of materials. Following Moore's law, much effort is put into continuously decreasing electronic feature dimensions. Indeed, typical feature sizes decreased from 10 µm in 1971 to 14 nm in 2014. The gradual shrinking of features thus entails a continuous improvement of the plasma processes. To go beyond 14 nm features, it is crucial to limit plasma induced damage (PID) during processing.

The etching of silicon or *low-k* material is often carried out by fluorine-containing plasmas because F atoms are the most reactive halides towards Si and SiO_2.

Recently, one novel process to limit plasma damage is cryogenic etching with $SF_6/O_2/SiF_4$ plasmas. During cryogenic etching with $SF_6/O_2/SiF_4$, the wafer is cooled to about -100 °C and a SiO_xF_y passivation layer condenses on the sidewalls of the etched trench, strongly reducing the diffusion of F atoms into the bulk and hence effectively limiting PID. The SiO_xF_y passivation layer evaporates at room temperature, leaving a clean trench with smooth sidewalls and no residues [1].

Cryogenic etching, although already proposed in 1988 [2], has recently seen an immense increase in popularity in microchip development, due to its very promising ability to reduce PID. However, this process is far from fully understood yet.

Here, we wish to obtain a fundamental understanding of the plasma behaviour and its interaction with the surface, to improve cryogenic plasma etching. For this purpose, we apply numerical models to describe the plasma behaviour for $SF_6/O_2/SiF_4$ plasma, and the surface interactions of the plasma species with the substrate. Furthermore, the modelling results are compared with experimentally measured etch rates for validation.

2. Modelling setup

The plasma simulations are carried out with a hybrid Monte Carlo - fluid model [3] to simulate the wafer-temperature-dependent etching of silicon. The bulk plasma in the inductively coupled (ICP) reactor volume as well as the surface reactions occurring at the wafer are self-consistently described.

Furthermore, MD simulations are carried out to obtain sticking probabilities, thermal desorption rates, surface diffusion rates and sputter yields of various fluorine-based species and their corresponding positive ions on Si(100) and on SiF_{1-3} surfaces, for different wafer temperatures ranging from 20 °C to -100 °C [4].

3. Experimental

Plasma etch experiments are carried out in an Alcatel 601E ICP reactor [5]. Etch rates are measured experimentally by reflectometry and directly compared with the calculated etch rates obtained from the simulations.

4. Results and discussion

The effects of the wafer temperature on the bulk plasma are investigated as well as the different surface behaviour during conventional etching and cryoetching.

It is observed that the etch rate increases when the wafer is cooled, when no or very low concentrations of oxygen are used. This is due to the local increase in gas density above the wafer since the gas is cooled here by the cold wafer. This, in turn, results in an increased flux of reactive F atoms and hence a higher etch rate. The lower local gas temperature above the wafer is illustrated in Fig. 1.

On the other hand, when a larger fraction of oxygen is applied to protect the sidewalls from lateral etching, the etch rate drops significantly if the wafer temperature is colder, as can be deduced from the experimentally measured etch rates shown in Fig. 2. This suggests that the formation of the SiF_xO_y passivation layer is enhanced at low surface temperature.

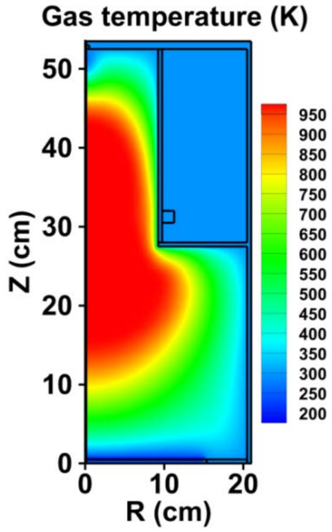

Fig. 1. Calculated average gas temperature in a half cross-section of the ICP reactor.

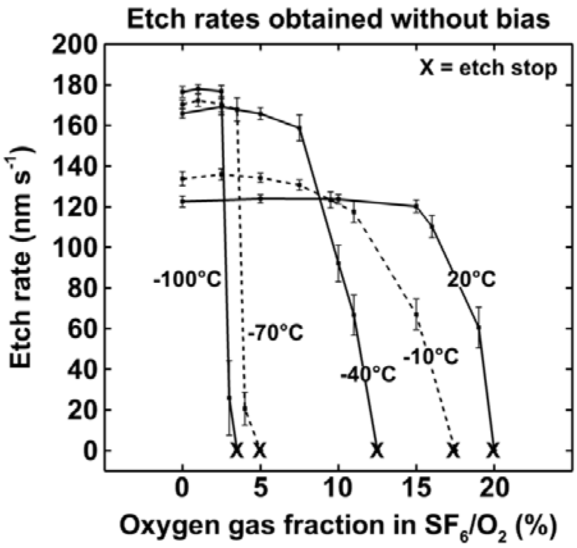

Fig. 2. Measured etch rates at different temperatures, as a function of O_2 fraction in the $SF_6/O_2/(SiF_4)$ plasma.

In the investigated pressure range of 1 to 9 Pa, the etch rate is always slightly higher at cryogenic conditions, both in the experiments and in the model, due to the local cooling of the gas above the wafer. The calculated and measured etch rates for 300 K and 173 K wafer temperatures as a function of pressure are illustrated in Fig. 3.

The MD simulations reveal that sticking and sputtering probabilities are almost not influenced by the wafer temperature in the range of 20 *°C* to -100 *°C*. The difference between cryoetching and conventional room temperature etching is found in the behaviour of physisorbed species.

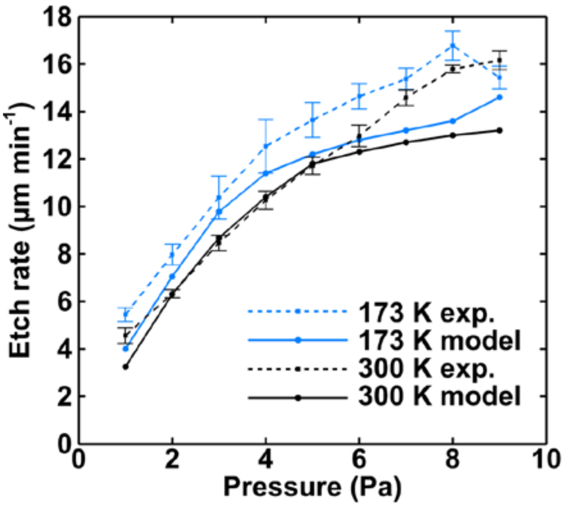

Fig. 3. Calculated and measured etch rates as a function of pressure for 300 K and 173 K wafer temperatures.

Indeed, thermal desorption occurs at a significantly lower rate at cryogenic conditions, which results in an accumulation of physisorbed species. As an example, the calculated desorption energies of various plasma species onto different SiF_x surfaces for both 173 K and 300 K are shown in Fig. 4.

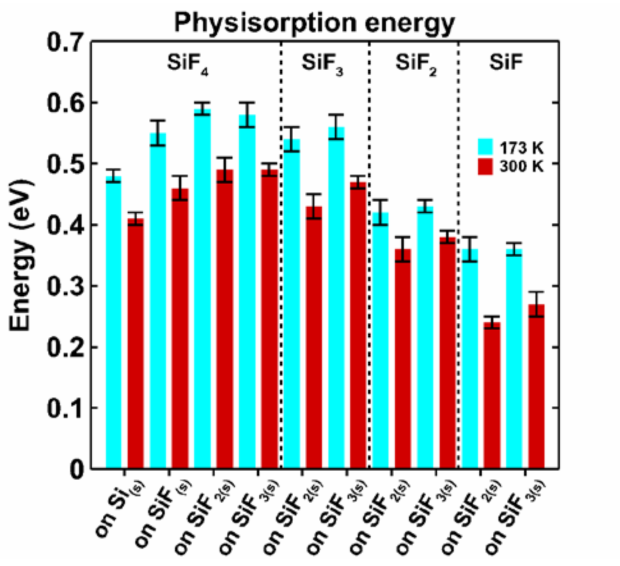

Fig. 4. Energy needed to desorb the physisorbed species from various SiF_x surfaces for 173 K and 300 K.

Thus, in the case of cryoetching, a physisorbed SF_x layer (x = 0 - 6) is formed on the wafer. The same layer is also formed at room temperature, but is not important, because of fast thermal desorption. However, in the case of cryoetching, the residence time of physisorbed species is long enough to entail accumulation of a physisorbed layer on top of the silicon wafer, as illustrated with physisorbed SiF_4 molecules on silicon in Fig. 5. This layer could not be formed with a significant thickness at room temperature, as is also illustrated.

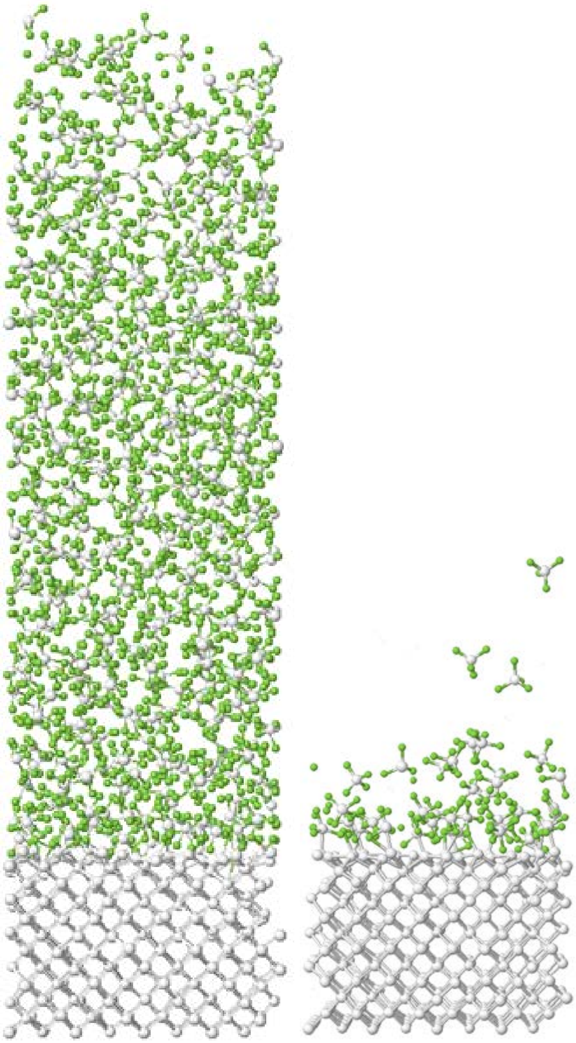

Fig. 5. Calculated accumulated layers of physisorbed SiF_4 molecules on Si(100) for 173 K (left) and 300 K (right).

However, even in the case of cryoetching, this layer can easily be disintegrated by low-energy ions, so it does not affect the etch rate at the bottom of the trenches or vias.

5. Conclusions

We have numerically and experimentally investigated an $SF_6/O_2/SiF_4$ low-pressure ICP, at different wafer temperatures ranging between 293 K and 173 K, to better understand the difference between cryoetching and room temperature etching. In this type of ICP reactor, where the plasma source is remote from the wafer, the bulk plasma is unaffected by the wafer temperature. Nevertheless, the etch rates are slightly higher at cryogenic temperature than at room temperature if no or minimal oxygen is used. Our plasma simulations indicate that this is caused by the local cooling of the gas above the wafer, resulting in a slightly denser gas and thus a higher density of reactive species, like F and F_2. This in turn entails a slightly higher flux of etching species towards the wafer, resulting in a slightly higher etch rate in the case of cryoetching.

Fundamental surface reactions are also investigated with MD simulations. It is found that the probabilities for chemisorption (i.e., sticking) and sputtering are almost not affected by the wafer temperature.

However, surface diffusion and thermal desorption of physisorbed species occur much slower at cryogenic conditions.

As a result, it is found that a thick layer of physisorbed species is formed during cryoetching, which is more or less absent at room temperature etching. This layer, however, has no effect on the etch rates because it is easily disintegrated by low-energy ions.

6. Acknowledgements

The Fund for Scientific Research Flanders (FWO) is acknowledged for financial support of this work. This work was carried out in part using the Turing HPC infrastructure at the CalcUA core facility of the Universiteit Antwerpen, a division of the Flemish Supercomputer Center VSC, funded by the Hercules Foundation, the Flemish Government (department EWI) and the University of Antwerp.

7. References

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