Study of substrate cooling mechanism of ICP dry etching system in non-silicon field

H. Ogiya, H. Nakano, K. Hasegawa, and O. Tsuji

Technical Department, Samco Inc., Kyoto, Japan

Abstract: Substrate cooling mechanisms are important in ICP dry etch systems. In the case of non-silicon materials such as GaAs, InP, GaN, glass, and sapphire substrates, it is necessary to provide strong adhesion force and coexist with various substrate sizes. This study reports on a unique implementation of a bottom electrode cooling mechanism using a JR-type electrostatic chuck that provides high suction force and an electrostatic suction tray that allows easy wafer size change and temperature control.

Keywords: ICP, RIE, ESC, JR-type, non-Silicon

1. Introduction

In dry etching systems using plasma, substrate temperature control is a core technology for process reproducibility. In dry etching, in addition to chemical etching by radicals from plasma generated in the gas phase, the etching process proceeds by physical etching in which ions are electrically accelerated to impact the substrate to be etched, and chemical reaction-accelerated etching by ion impact combining these two processes. The ion impact energy is converted into thermal energy of the substrate. Therefore, it is necessary to ensure sufficient heat conduction with the cooling stage where the etching substrate is installed. A well-known technique that can maintain substrate heat transfer without bonding the substrate is to fix the substrate to the stage and fill the gap between the substrate and the stage with helium gas. If it is possible to fill the gap of several 10 μm with He pressure of several thousand Pa, it is possible to transfer the substrate heat input of several 100 W to the lower stage within a temperature difference of several tens of degrees. At this time, the method of fixing the substrate is important.

Normally, the substrate is physically secured by clamps around the periphery, but the shadows of the clamps create areas where etching cannot take place. In addition, the center of the substrate is not secured, and the helium pressure causes a bulge the substrate, which tends to cause temperature distribution. In this case, an electrostatic chuck (ESC), which pulls the entire area onto the stage, is effective. An electrostatic chuck is a device that attracts a conductive substrate with electrostatic force by creating an electric potential in a thin electrode in an insulating substrate. In particular, in equipment that uses a high-density plasma source, such as ICP dry etching equipment, the temperature can easily rise to 200 to 300°C if the substrate is not cooled. Therefore, a substrate cooling mechanism with ESCs mounted on the bottom electrode is an important development element in pursuit of new processes.

This paper reports on a unique implementation of the bottom electrode cooling mechanism in ICP-RIE on non-silicon small-diameter wafers.

2. Experiment

The adsorption force F of an ESC corresponds to the Coulomb force of attraction between charges stored in the capacitor and can be expressed as in equation

$$F = \frac{1}{2}\varepsilon_0\varepsilon_r S\left(\frac{V}{d}\right)^2 \quad (1)$$

when the applied voltage is V, the electrode area is S, the distance between electrodes is d, and the relative permittivity of the dielectric layer is ε_r. This is a general expression for the adsorption force of Coulomb-type ESCs.

When the same voltage is applied, adsorption force is theoretically proportional to area, and if He pressure is the same, adsorption should be possible at the same voltage. However, empirically, the adsorption force tends to be lower for small-diameter wafers, and in the non-silicon field, it is necessary to ensure strong adsorption force for compound semiconductors and sapphire substrates, etc. Therefore, it is important to use Johnson-Rahbek effect type (JR-type) ESCs with conductive alumina as the dielectric [1-3]. The adsorption force F_{JR} of JR-type can be expressed as in equation

$$F_{JR} = \frac{1}{2}\varepsilon_0\left(\frac{V}{g}\right)^2 \quad (2)$$

when the distance d between electrodes in equation (1) becomes as small as the surface roughness and the gap is g. Since $g<<<d$, this indicates that the adsorption force of F_{JR} is very strong.

In the non-silicon field, it is necessary to support multiple substrate sizes with a single device, which basically means replacing ESCs of different diameters each time. However, since this requires a work process to change ESCs, it is necessary to consider simplifying the process. In this study, instead of placing the wafer in direct contact with the ESC, a unique method was developed in which a replaceable sheet is placed between the wafer and the ESC, both of which are clamped and cooled at the same time.

Fig. 1 shows the actual 4inch sheet. It is called an "ESC tray" because it is an electrostatically adsorbable tray. By

designing the surface according to the wafer size, it is possible to process wafers of different diameters at will on the same ESC.

However, as shown in equation (1), when the thickness of the tray is added, *d* increases, and the adsorption force drops sharply. Therefore, ESCs are made of conductive alumina with a volume resistivity of 10^9-10^{13} Ω･cm, and the same material was used for both ESCs and trays.

Fig.1 ESC tray for 4inch processing

An etching process was performed to confirm the ESC tray. The etching system used was a RIE-100HiC from Samco Inc. The high-density plasma source was an ICP system with 2000 W of 13.56 MHz applied, 300 W also applied on the substrate side, 3.0 Pa process pressure, 300 sccm of CF_4 gas, and 5% O_2 gas added as a polymer film removal gas. 1 μm thick thermal oxide (SiO_2) film deposited on a 4inch silicon substrate was continuously. The etching rate and in-plane distribution were measured. The wafers were electrostatically adsorbed with trays in the ESC, and He gas was filled between the wafers and trays, and between the trays and ESC, respectively. The same condition was applied to the wafers and the photoresist film, and they were evaluated in the same way. The photoresist film was used as an index to check the in-plane temperature stability because the etching rate varies greatly depending on the wafer surface temperature.

3. RESULTS AND DISCUSSION

The result of 500 wafers continuously is shown in Fig.2, where the etching rate of SiO_2 film is 1040nm/min and the etching distribution is about +/-1.0%, which is very stable while achieving high-speed etching. The flow rate of He to the ESC side is constantly monitored to confirm the adsorption force, and since it is also stable, it is judged that sufficient wafer clamping performance has been obtained.

As shown in Fig. 3(a), the etching distribution of the photoresist film tended to be higher at the outer edge of the wafer. By reviewing the introduction method of He gas, cooling performance was improved as shown in Fig. 3(b).

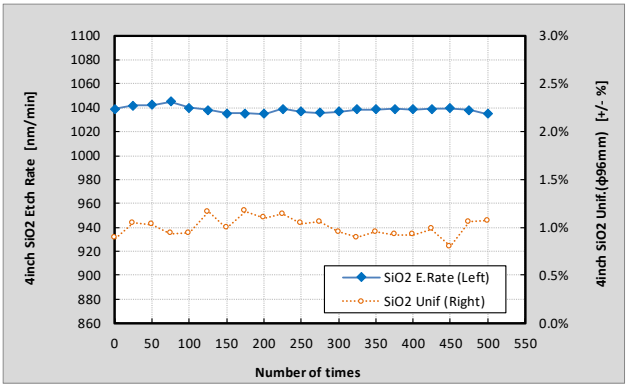

Fig.2. 500 consecutive etching results of SiO_2 film performed on ESC tray. Left: SiO_2 etching rate, Right: in-plane uniformity.

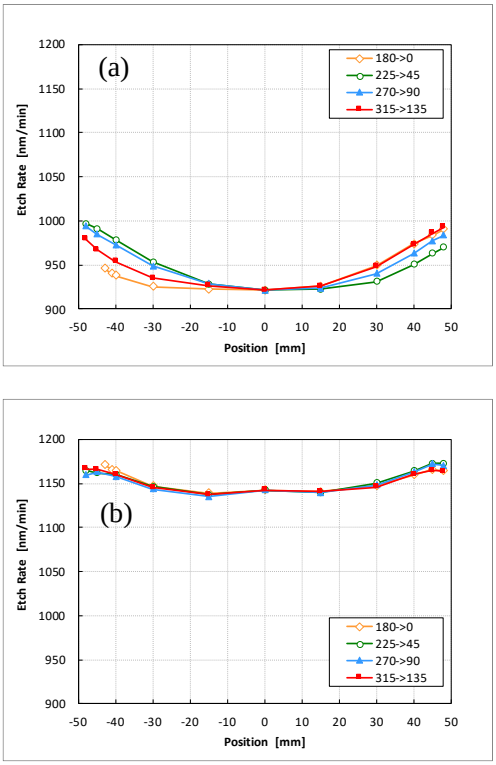

Fig.3. Detail of the etching distribution of the photoresist film performed in the ESC tray. (a) Conventional type, (b) Improved He gas introduction method on ESC side

4. Conclusions

We have developed a method to cool substrates of ICP dry etching equipment for non-silicon materials by clamping ESC and wafers together in the substrate cooling mechanism. The ESC tray is capable of electrostatic suction by taking advantage of the strong suction force.

The performance of the ESC tray was stable in terms of etching rate and uniformity even after processing 500 wafers continuously, so it can be judged that the adsorption

performance was stable and there was no effect on the process. However, by reviewing the He filling method, temperature stability has been achieved.

As a diversion of the technology, although it is not used in 8inch and 12inch substrate, the surface design of the ESC tray makes it possible to process a large number of wafers while cooling them, even in a batch system where multiple wafers are processed simultaneously at one time (Fig. 4).

Since the wear and tear of the trays and the method of static elimination are issues to be addressed, we will continue to study them.

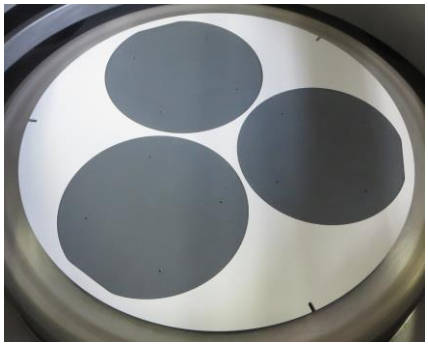

Fig.4 ESC tray for 3 4inch cards

5. References

[1] R. Atkinson, J. Phys. D: Appl. Phys, ser. 2, vol. 2, 325 (1969).
[2] G.I. Shim and H. Sugai, Plasma and Fusion Research. 3. 51-051 (2009).
[3] S. Qin and A. McTeer, J. Appl. Phys. 102, 064901 (2007).