PLASMA ETCHING OF HIGH-ASPECT-RATIO INTERCHIP VIAS FOR VERTICAL INTEGRATION OF CHIPS

M. Engelhardt

Siemens AG, Corporate Research and Development
Otto-Hahn-Ring 6, D-81730 Munich, Germany

Plasma processes were developed for deep trench etching in both dielectrics and single crystal silicon meeting the stringent requirements for fabrication of interchip vias with very high aspect ratios for Vertical Integration of Chips. After etching of vias with aspect ratios of typically 5:1 through a 6.5μm thick stack of passivation layers and all intermetal dielectrics of a 3-layer-metallization scheme, a subsequent deep silicon trench etching allows the fabrication of interchip vias as deep as 30μm with aspect ratios exceeding 20:1.

Introduction

Interchip vias are used for Vertical Integration of Chips (VIC) /1-3/. They provide the vertical connection of the uppermost aluminum lines of a thinned top wafer with those of a bottom wafer bonded to the back-side of the top wafer. Both wafers were submitted to a complete CMOS process and were carefully adjusted to each other during bonding. Interchip vias thus consist basically of a deep trench through the passivation layers and all intermetal dielectrics plus a deep trench through the single crystal silicon substrate of the thinned top wafer. For this study plasma etching of interchip vias was demonstrated using bulk silicon substrates.

Experimental

Both deep dielectric and silicon trench etching was achieved with magnetic field enhanced reactive ion etching (MERIE) using CHF_3/CF_4 and HBr/O_2 based etch chemistry respectively. Plasma etching of interchip vias was demonstrated with p-type silicon wafers with resistivities of 1-20Ωcm; they were 150mm in diameter and had [100] crystal orientation.

Results and Discussion

The dependence of the net resist etch rate on the gas mixture used for the dielectric etch shows (Fig. 1) that deep dielectric trenches (5.5-6.5μm) cannot be etched with low CHF_3 gas flows due to high resist loss. When a via etching process (CHF_3: 70%) commonly used for current memory and logic products is applied to deep dielectric trench etching, significant RIE lags were obtained due to high aspect ratios, with the etch rates for open areas (openings>10μm) being 3 times higher than for small diameter (1.4μm) vias; in addition profile tapering leading to CD changes was obtained. RIE lags were minimized with a modified process (CHF_3: 50%), by reducing the deposition of fluorocarbon films /4/ resulting in similar etch rates (400nm/min) for open areas and small diameter vias while maintaining sufficiently high selectivity to the photoresist mask to make use of standard single layer 2μm resist technology for pattern definition and transfer. The temporal evolution of dielectric trench profiles (Fig. 2) obtained with such a process shows etch rates independent on the aspect ratio and no profile tapering even when the dielectrics were completely etched through. SEM micrographs of as etched samples (Fig. 3a) demonstrate that the dielectric etch is highly anisotropic and provides sufficient sidewall protection to prevent lateral etch attack. Only after an addidional HF dip the individual dielectric layers can be seen (Fig. 3b). After deep dielectric trench etching and resist stripping, requiring no additional polymer removal steps, deep silicon trench etching follows, starting at the bottom of the dielectric trench. Using part of the passivation layers on top of the dielectric stack as hard mask, deep silicon trench etching was performed. This resulted in some tapering of the silicon trenches (Fig. 4). Tapering increases with increasing mask opening, with stronger taper being observed for grooves than for holes. This taper is due to thick redepositions (Fig. 5) on the via sidewalls; they consist of oxide formed during the silicon etch by a reaction of etch products with oxygen /5/. This type of tapering is therefore not observed when using thin oxide mask layers. The dependence of the profile taper on the type of structure and on the feature size can be explained straightforward with simple geometric considerations: Taking into account that the surface-to-volume ratio of a silicon trench is (by a factor of 2) smaller for grooves than for holes of similar depth and similar width, thicker films are deposited onto the sidewalls of grooves than of holes; further, by increasing the mask opening this ratio is further decreased, explaining the increase of the amount of deposited material and hence the increase of taper with increasing feature size. By reducing the silicon load on the wafers and optimizing the silicon trench etching process, almost vertical interchip vias were obtained (Fig. 6a, b) due to a controlled build-up of only very thin redepositions (Fig. 6c, d); these deep interchip vias (Fig. 6) were etched with non-uniformities of 2% and below. Our experiments show that the developed plasma etching processes have the capabilities for fabrication of interchip vias as deep as 30μm with aspect ratios exceeding 20:1 (Fig. 7).

Conclusion

Plasma etching of interchip vias for Vertical Integration of Chips (VIC) has successfully been demonstrated by a combination of deep dielectric and deep silicon trench etching.

Both depths and aspect ratios of the fabricated vias are exceeding those of vias in today´s most advanced DRAMs.

Acknowledgements

The author wishes to thank S. Schwarzl for valuable discussions. Special thanks are due to E. Renner for the SEM work and for technical assistance and to R. Braun for equipment support. VIC has been jointly developed by Siemens AG, Munich and the Fraunhofer Institut for Solid State Technology, Munich. This report is based on a project which has been supported by the German Minister of Research and Technology under the support-no O 1M 2926 B/C. For the contents the author alone is responsible.

References

/1/ E. Bertagnolli, H. Klose, P4400985.2 German Patent

/2/ P. Ramm, R. Buchner, P4433846.5, German Patent

/3/ M. Engelhardt, W. Pamler, B. Fröschle, T. Graßl, G. Ruhl, Proc. 7th Tegal Annual European Plasma Seminar, p. 13, (1995)

/4/ G. S. Oehrlein, Y. Zhang, O. Joubert, The Electrochem. Soc. Proc. Vol. 94-1, Abstract No. 222, p. 351, (1994)

/5/ M. Engelhardt, Proc. 10th Symp. on Plasma Processing, The Electrochem. Soc. Proc. Vol. 94-20, p. 224 (1994)

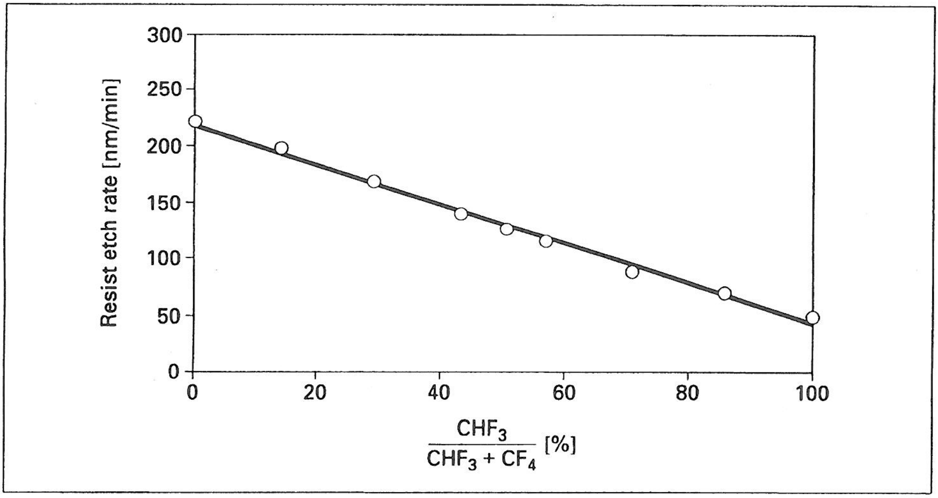
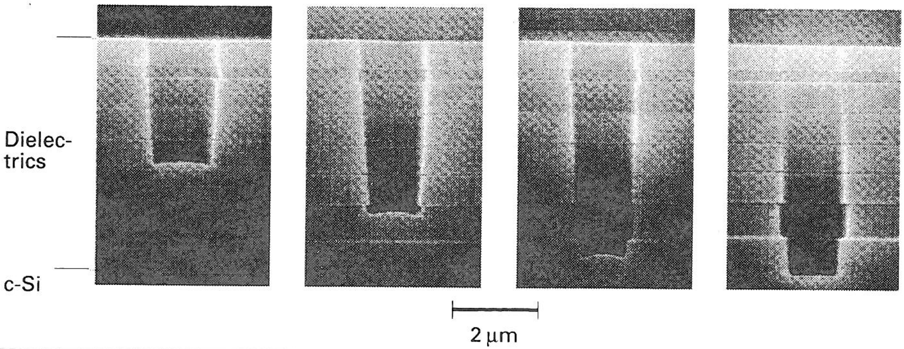


Fig. 1: Dependence of the net resist etch rate on the gas mixture used for the deep dielectric etch



Process Durantion [min]	7.5	10	12.5	15
Averaged Etch rate [µm/min]	0.39	0.40	0.40	> 0.37

Fig. 2: Temporal evolution of dielectric trenches (openings: 1.5μm; after HF dip) obtained with a process (CHF_3: 50%) with minimized RIE lags

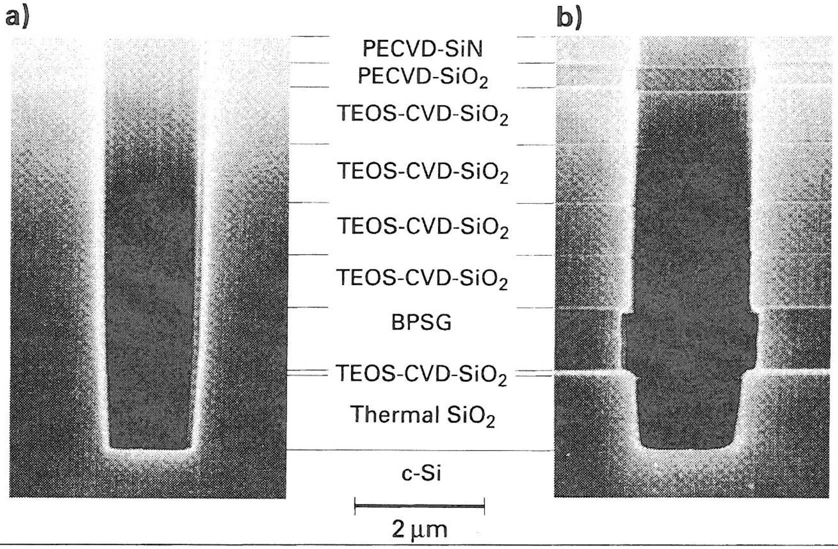


Fig. 3: Deep dielectric trenches through the passivation bi-layer and through all intermetal dielectrics of a 3-layer metallization scheme (a: as-etched, b: after HF dip)

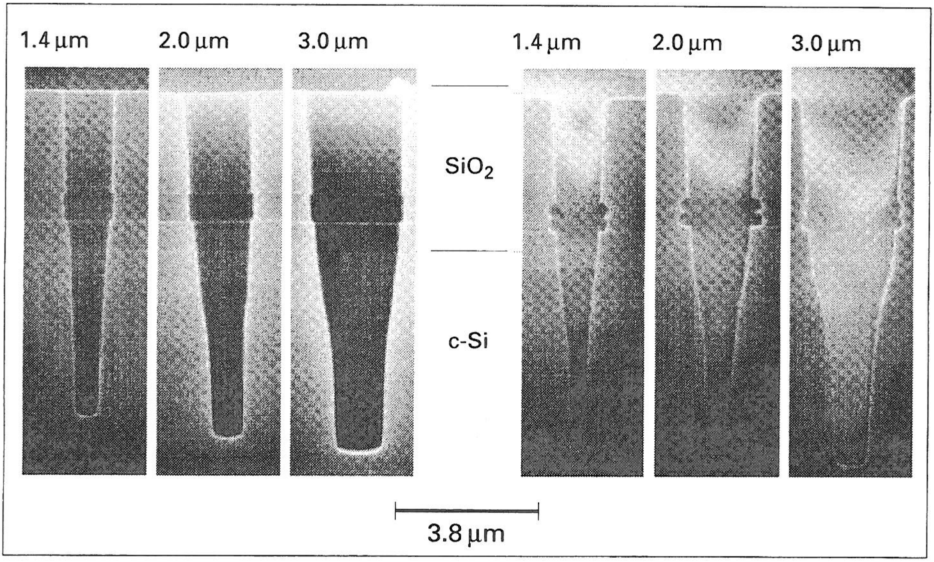


Fig. 4: Dependence of the profile taper on the openings of holes and grooves (after HF dip; see text!)

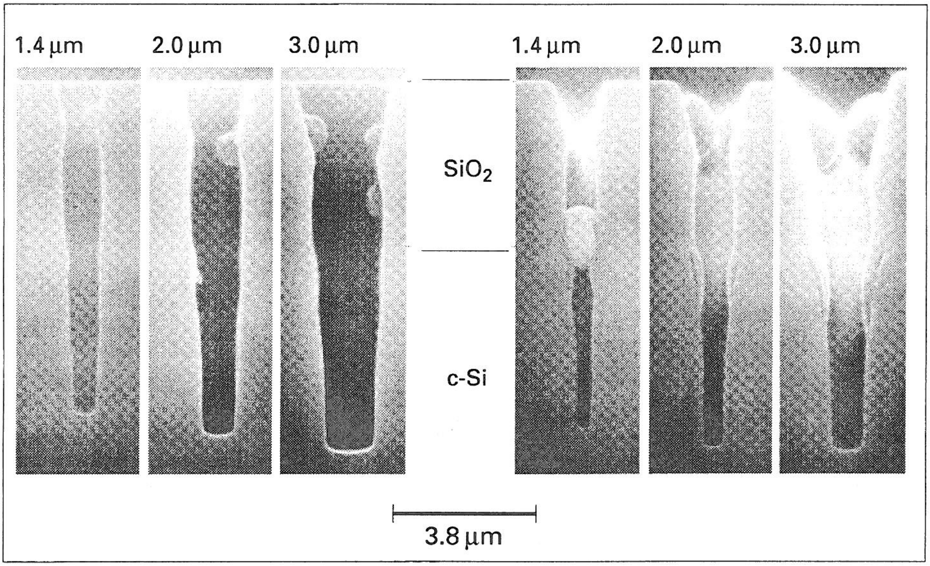


Fig. 5: Redepositions in the holes and grooves shown in Fig. 4 before applying an HF dip (as etched profiles; see text!)

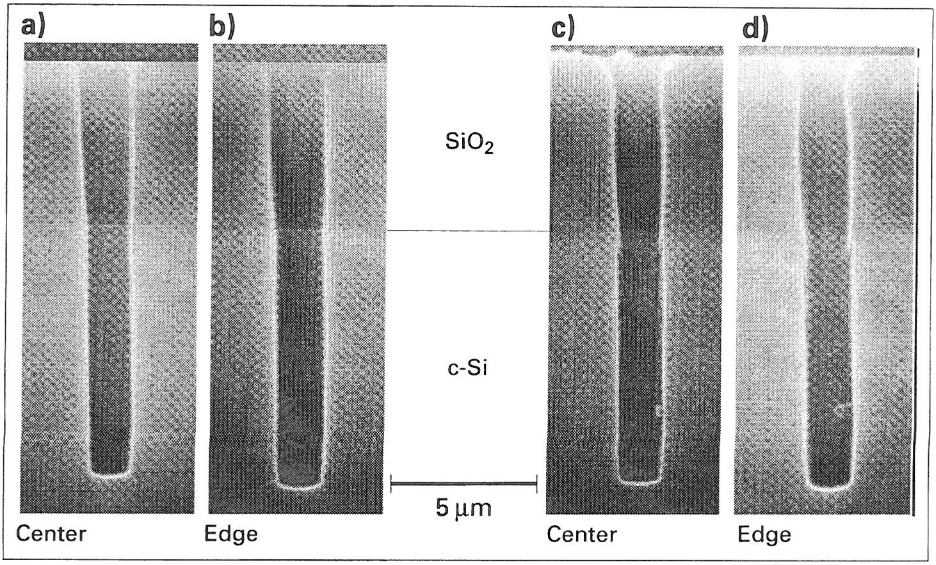


Fig. 6: Interchip vias with minimized profile taper (a, b: after HF dip) due to contolled build-up of only very thin redepositions (c, d: as etched) obtained with low etch rate non-uniformity across the wafer

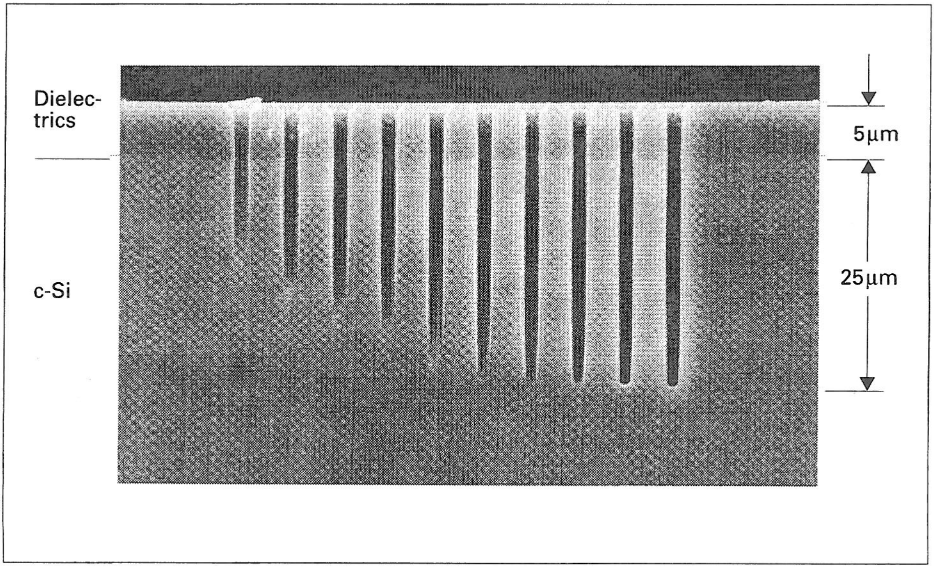


Fig. 7: Interchip vias with very high aspect ratio (>20:1) and an overall depth of 30μm